Ultrahigh Speed Pin Driver with Inhibit Mode

AD53040

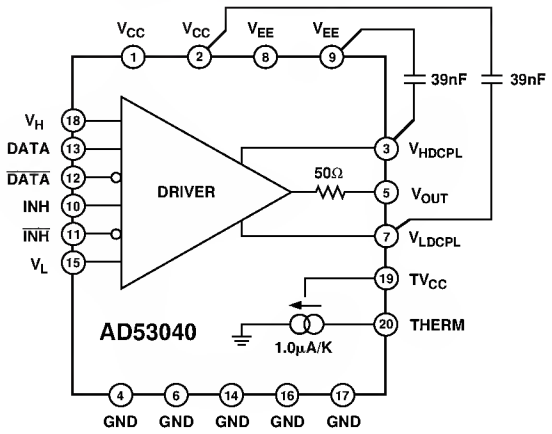
FEATURES

500 MHz Driver Operation
Driver Inhibit Function
100 ps Edge Matching
Guaranteed Industry Specifications
  50 Ω Output Impedance
  >1.5 V/ns Slew Rate
  Variable Output Voltages for ECL, TTL and CMOS
High Speed Differential Inputs for Maximum Flexibility
Ultrasmall 20-Lead SOP Package with Built-In Heatsink

APPLICATIONS

Automatic Test Equipment
  Semiconductor Test Systems
  Board Test Systems
Instrumentation and Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD53040 is a complete high speed pin driver designed for use in digital or mixed signal test systems. Combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long-term reliability in an ultrasmall 20-lead, SOP package with built-in heatsink.

Featuring unity gain programmable output levels of –3 V to +8 V with output swing capability of less than 100 mV to 9 V, the AD53040 is designed to stimulate ECL, TTL and CMOS logic families. The 500 MHz data rate capacity and matched output impedance allows for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (Inhibit Mode), electrically removing the driver from the path, through the Inhibit Mode feature. The pin driver leakage current inhibit is typically 100 nA and output charge transfer entering inhibit is typically less than 20 pC.

The AD53040 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry uses high speed differential inputs with a common-mode range of ±3 V. This allows for direct interface to precision differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 10 μA of bias current, the AD53040 can be directly coupled to the output of a digital-to-analog converter.

The AD53040 is available in a 20-lead, SOP package with a built-in heatsink and is specified to operate over the ambient commercial temperature range of –25°C to +85°C.

REV. 0

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AD53040–SPECIFICATIONS

(All specifications are at T_J = 85°C ± 5°C, $+V_S$ = +12 V ± 3%, $-V_S$ = –7 V ± 3% unless otherwise noted. All temperature coefficients are measured at T_J = 75°C–95°C). (A 39 nF capacitor must be connected between V_{CC} and V_{HDCPL} and between V_{EE} and V_{LDCPL}.)

Parameter	Min	Typ	Max	Units	Test Conditions
DIFFERENTIAL INPUT CHARACTERISTICS (DATA to $\overline{DATA}$, INH to $\overline{INH}$)					
Input Voltage		±3		Volts	
Differential Input Range		ECL			
Bias Current		±10		mA	V_{IN} = –2 V, 0.0 V
REFERENCE INPUTS					
Bias Currents	–50		50	µA	V_L, V_H = 5 V
OUTPUT CHARACTERISTICS					
Logic High Range	–2		8	Volts	DATA = H, V_H = –2 V to +8 V V_L = –3 V (V_H = –2 V to +6 V) V_L = –1 V (V_H = +6 V to +8 V)
Logic Low Range	–3		5	Volts	DATA = L, V_L = –3 V to +5 V, V_H = +6 V
Amplitude (V_H and V_L)	0.1		9	Volts	V_L = –0.05 V, V_H = +0.05 V and V_L = –2 V, V_H = +7 V
Absolute Accuracy					
V_H Offset	–100		+100	mV	DATA = H, V_H = –2 V to +8 V, V_L = –3 V
V_H Gain + Linearity Error		±0.3 ±5		% of V_H + mV	DATA = H, V_H = –2 V to +8 V, V_L = –3 V
V_L Offset	–100		+100	mV	DATA = L, V_L = –3 V to +5 V, V_H = +6 V
V_L Gain + Linearity Error		±0.3 ±5		% of V_L + mV	DATA = L, V_L = –3 V to +5 V, V_H = +6 V
Offset TC, V_H or V_L		0.5		mV/°C	V_L, V_H = 0 V, +5 V and –3 V, 0 V
Output Resistance	45	47	49	Ω	DATA = H, V_H = +3 V, V_L = 0 V, I_{OUT} = 30 mA
Dynamic Current Limit		150		mA	C_{BYP} = 39 nF, V_H = +7 V, V_L = –2 V
Static Current Limit		±65		mA	Output to –3 V, V_H = +8 V, V_L = –1 V, DATA = H and Output to +8 V, V_H = +6 V, V_L = –3 V, DATA = L
PSRR, Drive Mode		35		dB	V_S = V_S ± 3%
DYNAMIC PERFORMANCE, DRIVE (V_H and V_L)					
Propagation Delay Time		1.5		ns	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Propagation Delay TC		2		ps/°C	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Delay Matching, Edge to Edge		100		ps	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Rise and Fall Time					
1 V Swing		0.8		ns	Measured 20%–80%, V_L = 0 V, V_H = 1 V
3 V Swing		1.7		ns	Measured 10%–90%, V_L = 0 V, V_H = 3 V
5 V Swing		2.4		ns	Measured 10%–90%, V_L = 0 V, V_H = 5 V
Rise and Fall Time TC					
1 V Swing		±1		ps/°C	Measured 20%–80%, V_L = 0 V, V_H = 1 V
3 V Swing		±2		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 3 V
5 V Swing		±3		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 5 V
Overshoot, Undershoot and Preshoot		±(1% +50 mV)		% of Step + mV	a. V_L, V_H = 0.0 V, 1.0 V b. V_L, V_H = 0.0 V, 3.0 V c. V_L, V_H = 0.0 V, 5.0 V
Settling Time					
to 15 mV		40		ns	V_L = 0 V, V_H = 0.5 V
to 4 mV		8		µs	V_L = 0 V, V_H = 0.5 V
Delay Change vs. Pulse Width		25		ps	V_L = 0 V, V_H = 2 V, Pulse Width = 2.5 ns/7.5 ns, 30 ns/100 ns

Parameter	Min	Typ	Max	Units	Test Conditions
DYNAMIC PERFORMANCE, DRIVE (V_H and V_L) (*Continued*)					
Minimum Pulse Width					
3 V Swing		1.7		ns	4.0 ns Input, 10%/90% Output, V_L = 0 V, V_H = 3 V
5 V Swing		2.6		ns	6.0 ns Input, 10%/90% Output, V_L = 0 V, V_H = 5 V
Toggle Rate		500		MHz	V_L = –1.8 V, V_H = –0.8 V, V_{OUT} > 600 mV p-p
DYNAMIC PERFORMANCE, INHIBIT					
Delay Time, Active to Inhibit	2		5	ns	Measured at 50%, V_H = +2 V, V_L = –2 V
Delay Time, Inhibit to Active	2		5	ns	Measured at 50%, V_H = +2 V, V_L = –2 V
I/O Spike		<200		mV, p-p	V_H = 0 V, V_L = 0 V
Output Leakage	–1.0		+1.0	µA	V_{OUT} = –3 V to +8 V
Output Capacitance		5		pF	Driver Inhibited
POWER SUPPLIES					
Total Supply Range		19		V	
Positive Supply		+12		V	
Negative Supply		–7		V	
Positive Supply Current			75	mA	
Negative Supply Current			75	mA	
Total Power Dissipation		1.15	1.43	W	
Temperature Sensor Gain Factor		1.0		µA/K	R_{LOAD} = 10 K, V_{SOURCE} = +12 V

NOTES
Connecting or shorting the decoupling capacitors to ground will result in the destruction of the device.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND ..... +13 V
- $-V_S$ to GND ..... –8 V
- $+V_S$ to $-V_S$ ..... +20 V

Inputs
- DATA to $\overline{DATA}$, INH to $\overline{INH}$ ..... +5 V, –3 V
- DATA to $\overline{DATA}$, INH to $\overline{INH}$ ..... ±3 V
- V_H, V_L to GND ..... +9 V, –4 V
- V_H to V_L ..... +11 V, 0 V

Outputs
- V_{OUT} Short Circuit Duration ..... Indefinite[2]

V_{OUT} Range in Inhibit Mode
- V_{HDCPL} ..... Do Not Connect Except for Cap to V_{CC}
- V_{LDCPL} ..... Do Not Connect Except for Cap to V_{EE}
- THERM ..... +13 V, 0 V

Environmental
- Operating Temperature (Junction) ..... +175°C
- Storage Temperature ..... –65°C to +150°C
- Lead Temperature (Soldering, 10 sec)[3] ..... +260°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Output short circuit protection is guaranteed as long as proper heatsinking is employed to ensure compliance with the operating temperature limits.
[3]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ± 5°C (75°F ± 10°F) with relative humidity not to exceed 65%.

ORDERING GUIDE

Model	Package Description	Shipment Method, Quantity Per Shipping Container	Package Option
AD53040KRP	20-Pin Power SOIC	Tube, 38 Pieces	RC-20

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53040 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

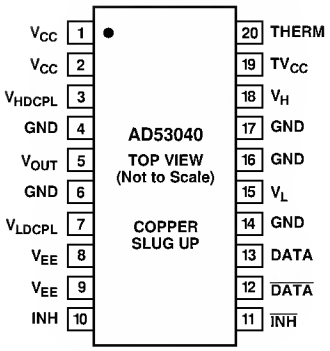


Table I. Pin Driver Truth Table

DATA	$\overline{DATA}$	INH	$\overline{INH}$	Output State
0	1	0	1	V_L
1	0	0	1	V_H
0	1	1	0	Hi-Z
1	0	1	0	Hi-Z

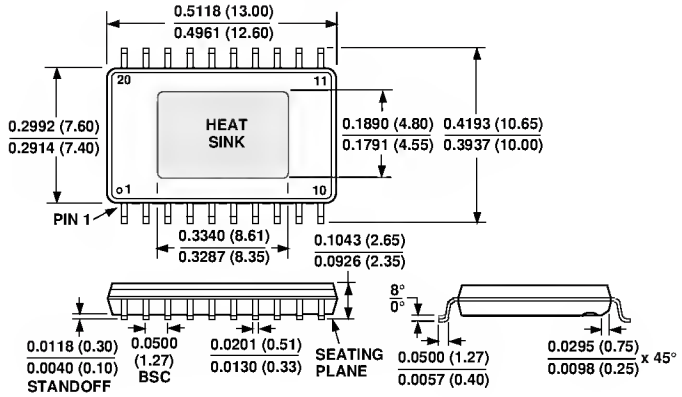
Table II. Package Thermal Characteristics

Air Flow, FM	θ_{JC}, °C/W	θ_{JA}, °C/W
0	4	50
50	4	49
400	4	34

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Thermally Enhanced Small Outline Package (PSOP) (RC-20)



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